Discrete Optimization of EMI Filter Using a Genetic Algorithm

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***Abstract*—A discrete optimization using a genetic algorithm (GA) for electromagnetic interference (EMI) f ler design is presented in this paper. Using a macro-model in the frequency domain this approach takes into account the load impedance and the source emissions. The macro-model includes an accurate f lter model that takes into account the PCB stray elements and the passive components high frequency complex behavior. A framework between on two software is established. This framework permits a data exchange between the f lter accurate model and the GA algorithm. This approach is applied on a Class-D amplif cation system for validation. Using the suppliers well-def ned surface mounted devices (SMD) database, the GA search for a set of components that respects the Electromagnetic Compatibility limits while reducing the f lter power losses.**

***Index Terms*—Discrete optimization, Electromagnetic compatibility, Filter design, Genetic algorithms, Class-D amplif er.**

I. Introduction

Nowadays, smart-phones became very complex systems that include numerous applications for everyday use, and reducing their power consumption is a major challenge to increase the device autonomy. With an eff ciency around 90%, Class-D audio amplif ers present a good solution for the hands-free audio applications. A Class-D amplif er is a switching device composed by a switching power stage controlled by Pulse Width Modulation (PWM). With a switching frequency around 400 kHz, a rise/fall time around 10ns and delivering a current up to 1 A peaks, a Class-D amplif er is a serious source of Electromagnetic Interference (EMI) in portable cell-phones. Thus, EMI f lters are mandatory to protect the surrounding electronics from the high disturbance level.

EMI f lters are added in order to improve the Electromagnetic Compatibility (EMC) of the system. Designing the EMI f lters can be very challenging because their performance highly depend of the parasitic components. Moreover, these f lters have an impact of the f nal application which is often undesirable. In the case of Class-D amplif ers, EMI f lters are able to increase the power losses in the amplif er and attenuate the amplitude of the audio signal at the load. These negative effect are rarely taken into account while designing an EMI f lter.

Some EMC experts rely on the experience to design the EMI f lter. Other designers refer to the classical f lter design methodology which consists of determining the required attenuation of conducted emissions relative to a given EMI standard or system specif cation, then computing the values of inductances and capacitances analytically for a given topology [1], [2]. These procedures may lead to sub-optimal solutions for goals such as volume, area or electrical consumption. Thus, the f lter design formulated as an optimization problem can be advantageous.

A continuous optimization has been applied to EMI f lter design for power electronics [3]–[5], for aerospace applications [6], [7] and for signal processing [8]. However, in integrated micro electronic applications such as mobile phones, continuous optimization is less adapted. Passive f lters in this case are constituted of surface mounted devices (SMD). SMD passive components have a well def ned nominal values available in the market. Components nominal values given by a continuous optimization are most of the time not available among suppliers.

The number of available components in the market considering all suppliers is very high. For instance, a f lter of 5 elements and 1000 components per element, which is a fairly small problem, corresponds to a discrete design space of size $(10^3)^5 = 10^{15}$. Considering that each function evaluation takes about 10s, the time required for an exhaustive search would be of the order of hundreds of millions of years. This fact strongly motivates the use of optimization.

Previous work such as [9]–[13], neglect or give less importance to the parasitic effects of components and printed circuit board (PCB) tracks. Nevertheless, this part is essential in high frequency EMI modeling. In [14], the equivalent series

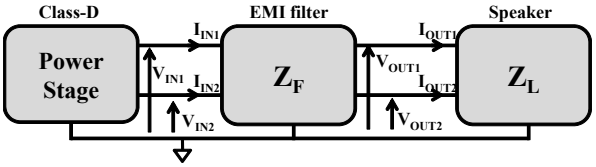

Fig. 1. Amplification system block diagram.

resistance, capacitance and inductance of SMD components are modeled with lumped circuit elements as an attempt to increase accuracy in EMC analysis and optimization. However, there's no simple expression that links these parasitic effects to the component nominal value.

This paper proposes a filter design based on discrete optimization by Genetic Algorithms (GA) and a system model based on three different approaches. The first approach is a system macro-modeling technique presented in [15], [16] that takes into account the system imperfection, the source emissions and the load impedance for Electromagnetic (EM) emission computation. The second approach is the filter model which is implemented in Advanced System Design (ADS) software. It takes into account most of the filter imperfections such as the Printed Circuit Board (PCB) layout and PCB stray components. The third approach is a library of ADS models for SMD passive components provided by the supplier. The optimization loop is implemented in MATLAB and it is used to search for a set of components among suppliers libraries that minimizes the optimization objectives.

Section II presents the used modeling approach. Section III explains the optimization methodology. Section IV presents the application on a Class-D amplification system. Finally, section V conclude by resuming the basic ideas of this paper.

II. EMI Modeling

The frequency model presented in [15], [16] has been used for system modeling. This model is chosen mainly because it deals with differential systems such as the integrated Class-D amplifiers. This approach is particularly interesting to study the filter in the final application, according to a specific EMI source and load with a good accuracy at high frequencies. In addition, this model has a short simulation time. Thus, this model integrated in an optimization loop, can be used to EMI filter design by optimization.

A. Modeling approach

The considered approach consists on decomposing the system into functional blocks, as shown for the case of a Class-D amplifier in Fig. 1. The filter and the load are modeled by impedance matrices and the amplifier is modeled by electric sources and an impedance matrix, that correspond to the converter output impedance. However, in this case the converter output impedance is negligible and it has been proved in [15]. The load impedance matrix can be measured or simulated. In this work, it has been measured using an impedance analyser. The modeling approach proposes three different methods (impedance matrix, vector network analyser or simulation) to determine the filter impedance matrix. In this paper the simulation method is the most interesting since the main purpose is the filter optimization before construction.

B. Filter model

The filter high frequency behavior depends on the filter parasitic stray elements. Therefore, a fixed filter topology has been implemented in Advanced Design System (ADS) [17]. The model includes the filter layout design and all the PCB physical characteristics. Thus, the stray elements related to the filter layout such as track impedances are taken into account. In the filter model, the SMD components have been replaced by their dedicated model for ADS which is provided by the suppliers. Hence, the passive components stray elements related to the technology and the packaging of each component is taken into account. Finally, ADS generate an impedance matrix including most of the filter stray elements and imperfections for more accuracy at high frequencies. This impedance matrix is used in the macro-modeling presented in the previous sub-section.

C. Currents and voltages computation

Using the impedance matrices and the converter output voltages in the frequency domain, the current and voltages at all the system nodes can be computed. Note that the converter output voltages must be measured in the time domain then converted to the frequency domain by a Fast Fourier Transformation (FFT) to conserve a correct phase at all the frequencies. The modeling and the calculation details are not presented in this paper for the sake of simplicity, but they can be found in [15], [16]. The computation generates vectors of currents or voltages on each frequency from the considered frequency vector, to be used in the filter optimization algorithm.

III. Methodology

Designing an EMI filter can be summarized by two major steps:

- determine a filter topology,
- choose the components.

Generally, the filter structure can be found by using common structures in the literature, or in some cases, complex design can be done following the specifications of the application itself. Here, the EMI filter topology and component values found in the literature for Class-D amplifiers has been used as a reference [18]. The filter topology is presented in Fig. 2 and the component values are presented in Table I. With a fixed topology, the challenge in the optimization becomes the choice of the components from the supplier's libraries, in order to increase the efficiency of the filter.

SMD suppliers provide models for SMD components classified in libraries and dedicated to ADS. Two different libraries have been utilized for this case of study. The first is muRata's library for SMD capacitors (718 capacitors). The second one is TDK library for SMD inductors (8 inductors). These libraries have already been sorted based on constraints of minimum supported current by inductors, maximum supported voltage

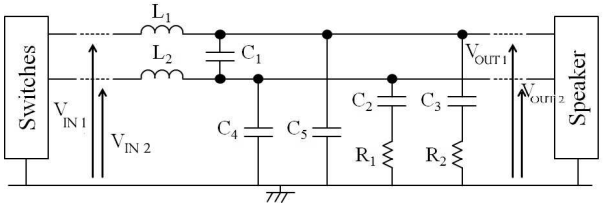

Fig. 2. Filter topology.

TABLE I
FILTER COMPONENTS VALUES.

L_1, L_2	$15\mu H$	Ref TDK: CLF7045T-150M
C_1, C_2	$0.033\mu F$	Ref muRata: GRM155R61A683KA01
C_4, C_5	$0.068\mu F$	Ref muRata: GRM155R61A683KA01
C_3	$0.15\mu F$	Ref muRata: GRM155R61A154KE19
R_1, R_2	22Ω	no particular supplier considered

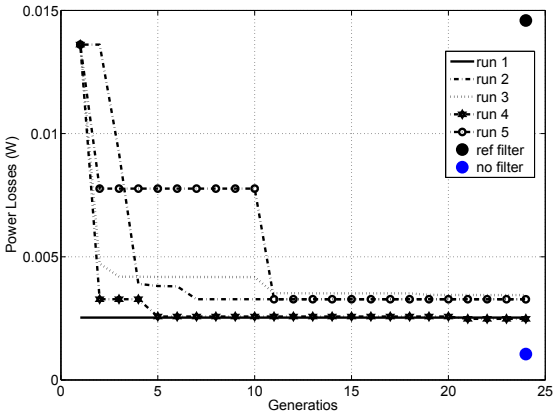

Fig. 3. Convergence of Optimization loop.

by capacitors and the component footprint size. In MATLAB enviroment, a genetic optimization algorithm was implemented and a correspondent database of SMD components was created. Then, a framework of data exchange between MATLAB and Agilent ADS was developed. The process is described as follows:

1) a MATLAB script generates an Agilent ADS netlist file containing indexes of components in a previously installed supplier database (inductors, capacitors and resistors),
2) a command invokes ADS to simulate the netlist created,
3) ADS reads the netlist and executes a simulation,
4) An output file containing the Z-parameters of the filter is created,
5) a MATLAB script reads the file created by ADS.

In order to designing a high quality EMI filter, the filter optimization should focus on the following aspects:

- do not exceed the EMI limits defined by the user
- minimize the filter power losses
- respect a maximum area on the PCB
- keep a minimum level of audio attenuation at the speaker level

Therefore, based on the system requirements and optimization expertise, the formulation of the optimization is made as follow.

First, minimizing the power losses introduced by the filter is set as the optimization objective. Second, the EMI, the area on PCB and the audio attenuation criteria are set as constraints. The output current spectrum of the optimized filter must not exceed the one when using the reference filter. The component footprints are fixed as the same ones as the reference filter. The reason is to keep the same PCB layout of the original filter. Finally, the audio signal at the load should not be attenuated more then $2.5\,\%$ when compared to the one when no filter is used. Note that the constraints are introduced as penalties in the objective function which is given by (1).

$$Obj = Min(P_{losses} + EMI_{penalty} + Audio_{penalty}) \quad (1)$$

P_{losses} is the filter power losses and is given by the following expression:

$$P_{losses} = P_{Class-D} + P_{FL} - P_{Audio} \quad (2)$$

where $P_{Class-D}$ is the power losses inside the Class-D amplifier, P_{FL} is the active power of the filter and load together, which is seen by the Class-D amplifier, and P_{Audio} is the audio delivered power. $P_{Class-D}$, P_{FL} and P_{Audio} are computed directly in the frequency domain by the following three expressions respectively.

$$P_{Class-D} = R_{ds-on} * (I^2_{IN1-rms} + I^2_{IN2-rms}) \quad (3)$$

$$P_{FL} = Re(V_{IN1} * I^*_{IN1}) + Re(V_{IN2} * I^*_{IN2}) \quad (4)$$

$$P_{Audio} = Re((V_{Audio}) * (I_{Audio})^*) \quad (5)$$

where R_{ds-on} is the internal resistance of the Class-D amplifier, V_{IN1} and V_{IN2} are the amplifier input voltages, I_{IN1} and I_{IN2} are the amplifier input currents, V_{Audio} is equal to $V_{OUT1} - V_{OUT2}$ at the audio frequency and I_{Audio} is equal to I_{OUT1} (or $-I_{OUT2}$) at the audio frequency.

IV. APPLICATION

The methodology described in the last section has been applied to the design of an EMC filter, with the topology shown in Fig. 2. The problem consists of choosing the components R_1, L_1, C_1, C_3 and C_5, knowing that by symmetry, R_2, L_2, C_2 and C_4 are automatically chosen.

The optimization algorithm used was a discrete version of the GA's native implementation in MATLAB. Five executions of the optimization were performed, leading to similar results, which are shown in Fig. 3.

Note in Fig. 3, that the reference filter, the optimized filter after 25 generations and the no-filter case have power

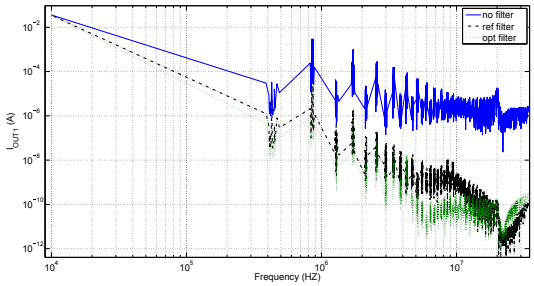

Fig. 4. Comparison of current spectra I_{OUT1}

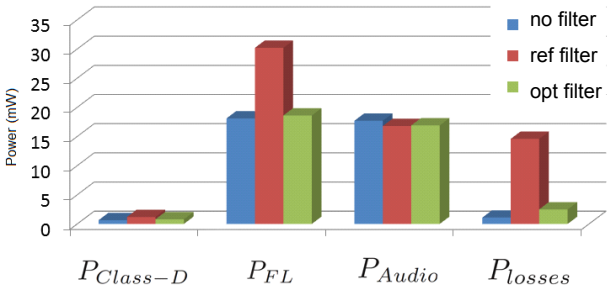

Fig. 5. Comparison of Power

losses of around 15mW, 2.5mW and 2mW respectively. This means that the optimized f lter has approximately 6 times less power losses than the reference f lter, for the same EMI level and components area. Moreover, the optimized f lter's losses approached the no f lter case, which, from the designer point of view, means introducing an extra passive component without increasing signif cantly the power losses.

In Fig. 4, the current spectra for the cases no f lter, reference f lter and optimized f lter is presented. Note that, the optimized f lter is slightly better in EMC than the reference f lter, even though this was a constraint and not an objective.

Fig. 5 presents a power analysis, describing each contribution of expressions (3), (4) and (5) to the total losses. Note that the power losses in the Class-D amplif er are negligible compared to the losses in the f lter. This fact motivates a more careful choice of f lter components for higher eff ciency.

In Table II, it is shown the optimized components list.

V. Conclusion

In this paper, an EMC f lter design by discrete optimization was presented. A comparison of the optimized f lter and a reference f lter showed, for the considered application, that the optimization methodology proposed a f lter with around 6 times less power losses than the reference, with the same EMI behavior and PCB area. Thus, the relevance of the proposed method became evident. Moreover, at the end of the optimization loop, the designer is able to order the optimized components directly, since the result of the method is an optimized list of components. This will be the future work for an experimental validation.

TABLE II
Optimized Filter component values.

L_1, L_2	$22\mu H$	Ref TDK: CLF7045T-220M
C_1, C_2	$0.47\mu F$	Ref muRata: GRM155R60J474KE19
C_4, C_5	$1.2pF$	Ref muRata: GRM1535C1H1R2CDD5
C_3	$0.1\mu F$	Ref muRata: GRM155R61H104KE19
R_1, R_2	1.6Ω	no particular supplier considered

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