Conducted EMC Prediction for a Power Converter with SiC Components

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Abstract — **This paper presents a model of a power converter with SiC components in order to predict the conducted perturbation that it generates (at the LISN level). Some methods to create a model of any passive elements (parasitic capacitance and inductance, decoupling capacitors, load, LISN) as an equivalent circuit are shown. Finally the complete model of the converter is presented and confronted to experimental measurements. Comparisons show a good behaviour until 30MHz.**

I. Introduction

The recent technological progress of semiconductors and increasing demand for electronic power converters with new specifications such as high frequencies, high voltages, high temperatures and strong current densities propose SiC (Silicon Carbide) components as an adapted solution. The use of these components generates new issues in Electromagnetic Compatibility (EMC) because of the conditions of high frequency switching and high commutation speeds (high di/dt and dv/dt) compared to other components in power electronics. A precise study of the perturbations generated by the SiC components hasn't been conducted yet.

The aim of this work is to predict the levels of conducted emission generated by electronic power converters fitted with SiC components allowing a reduction of costs in the phase of development.

A realistic model for (EMC) must identify and model all the parasitic elements [1,2]. It's equally necessary to have a model of semiconductor devices. In order to predict compliance to EMC standard, a LISN (Line Impedance Stabilization Network) must be included in the model.

In this paper a buck converter is considered (Fig. 1). The active components (i.e. disturbances sources in EMC) are a Si Schottky diode (MUR1540) and a SiC JFET manufactured by SiCED/INFINEON Company. The model used for the diode is provided in the Saber® [3] library. The JFET model was developed in [4].

In section II, passive components are modelled with equivalent electrical circuits. The non idealities considered are the load imperfections, the decoupling capacitors imperfections, the LISN, parasitic inductive effects in tracks and capacitive effects between track and ground plane.

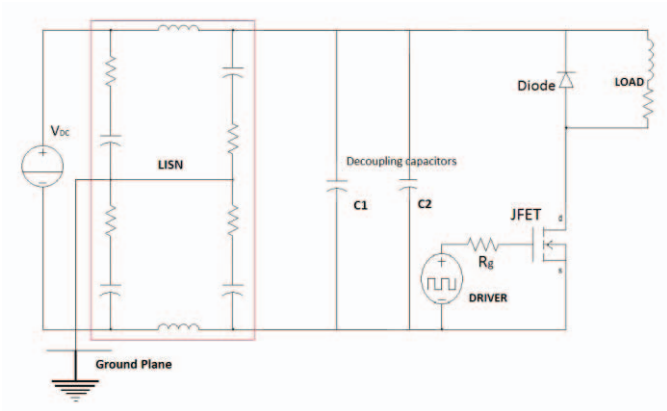

Fig. 1 Considered converter

In section III, the model is compared with measurements. Firstly, the model including all parasitic components is compared with impedance measurements. Secondly the current across the load is predicted in the Saber® simulation environment (time domain) and compared with the measurements. Finally conclusions and perspectives are presented.

II. Passive and Parasitic Components Modelling

A. Passive components

For the passive components (decoupling capacitors, load and LISN) an impedance meter AGILENT 4294A was used to extract the frequency behavior of each component.

An optimization algorithm (written in MATLAB) is used to compute the parameters of a proposed electrical model (deduced from the frequency behavior of the component) in order to minimize the difference between the impedance of the model and measurement.

Fig. 2 shows the measurements performed with the impedance meter for the load, compared with results of the simulation obtained by the equivalent circuit model.

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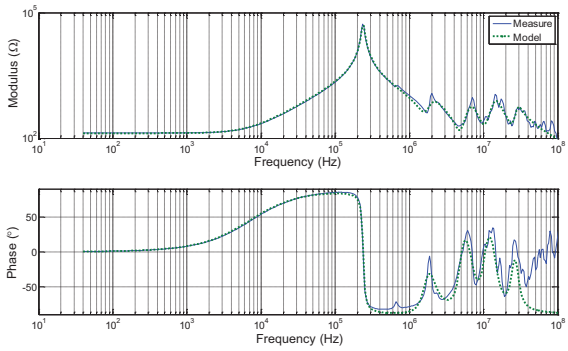

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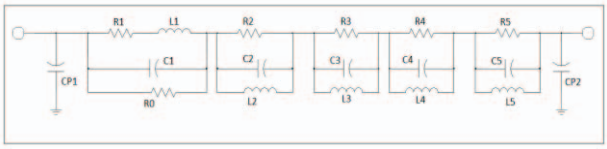
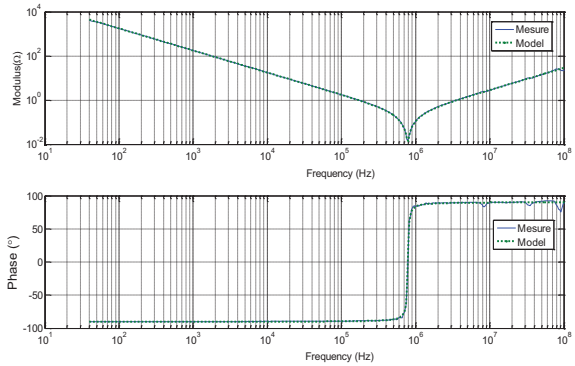


(b)

Fig. 2 Load model (a) impedance measure and simulation (b) model

For the converter, two decoupling capacitors are used: an electrolytic capacitor (C1) and a ceramic capacitor (C2). The electrical model used for decoupling capacitors is a circuit R-L-C series (Fig. 3).



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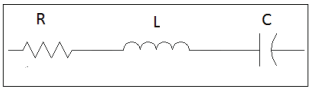
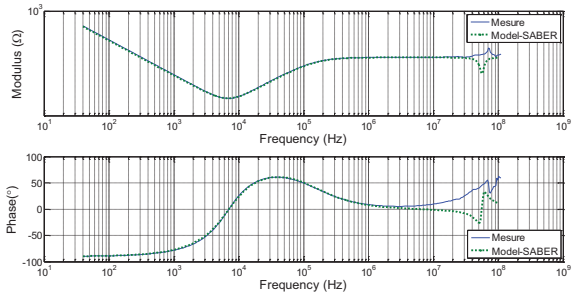


(b)

Fig. 3 Decoupling capacitor (a) impedance measure and simulation (b) model

The LISN used is a "50A: Prana Tegam-50 Ohms-50uH". Its schematic is represented in Fig. 1. Each component was measured and the equivalent circuit model has been developed (Fig. 4).



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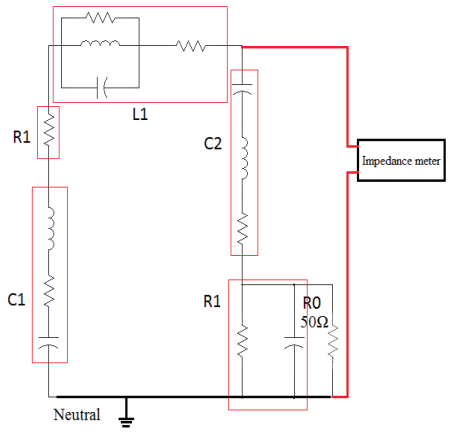


(b)

Fig. 4 LISN model (a) impedance measure and simulation (b) model

We can observe a good agreement between measurements and models until 30MHz.

B. Parasitic elements

B.1 Inductive effects

The cabling model is very important in the converter design; it is responsible for the over-voltage in the switches terminal due to the high di/dt and dv/dt generated during the commutation step.

The coupling inductances, the skin effect and the proximity effect produce supplementary losses in the conductors that can be limited by changing the form and the positioning between conductors.

The effects named previously are taken into account by modelling the tracks of the PCB with InCa3D® software [5]; this version models only the inductive and resistive aspects based on PEEC method (Partial Element Equivalent Circuit) [6]. This approach allows modelling the non ideal behaviour of cooper tracks.

To observe the cabling influence in the converter behaviour, asymmetric and long tracks are proposed. With this design the disturbing effects are higher in the considered bandwidth. The circuit simulated is presented Fig. 5.

InCa3D® generates a matrix of impedance and the differential equations using MAST language that is exported to Saber®.

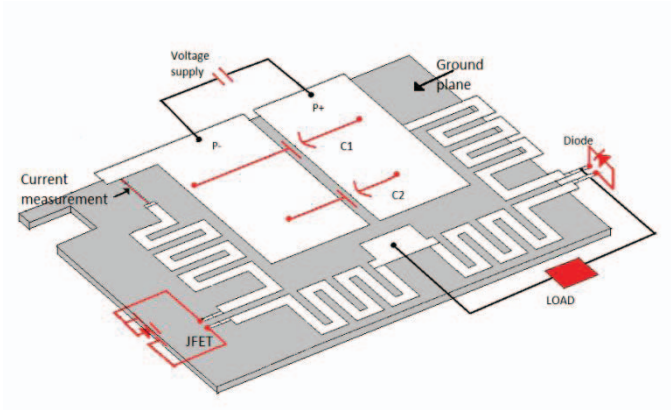


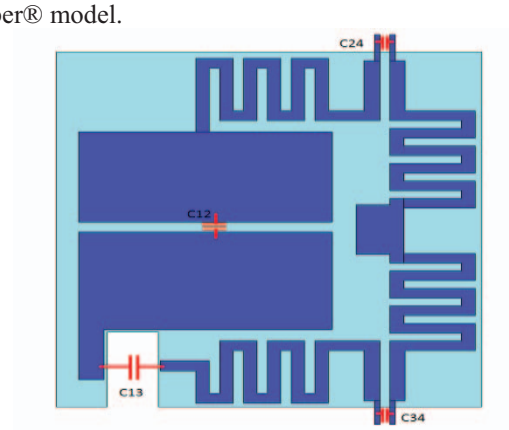
Fig. 5 Circuit geometry

B.2 Capacitive effects

The stray capacitance offers a path to the common mode current. Four stray capacitances between tracks (Fig. 6a) and four between tracks and ground plane (Fig. 6b) are considered. The values of parasitic capacitance depend on the geometry of the physical structure, three formulations of the literature are used for the calculation [7] and compared to measurements with the impedance meter.

These capacitances can not be directly measured. Indeed when the impedance meter is placed between two points, it measures several capacitances associated in series and/or in parallel. Then an adapted methodology has been used to obtain capacitance values. It consists of making short-circuits and open-circuits between the cooper tracks. The impedance meter measures equivalent values to correspond to lineal equations of the stray capacitances between tracks and stray capacitances between tracks and ground plane. The resolution of this set of equations gives the stray capacitances values.

Finally, the method that gives better results is Sakurai and Tamaru formula. This formula take into account edge effects [7]. Stray capacitances between tracks are negligible compared to the capacitances between tracks and ground plane [8]. Then only four stray capacitances are integrated to the Saber® model.



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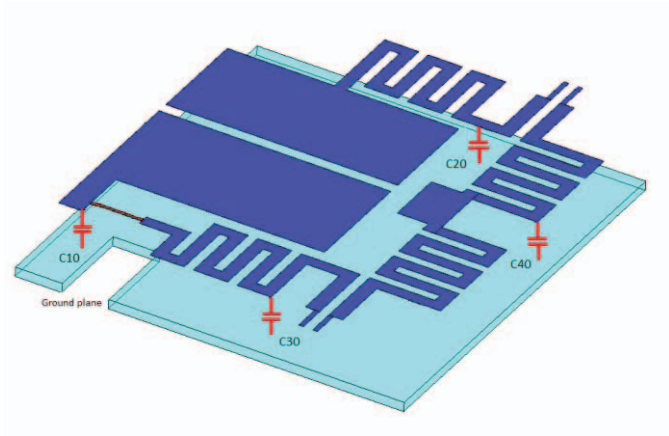

(b)

Fig. 6 Circuit geometry (a) stray capacitances between tracks (b) stray capacitances between tracks and ground plane

III. Validation of the Model

A. Simulated impedance compared with measurements

To validate the model, measurements of impedance are made and confronted with the model in Saber®; all the parasitic elements are taken into account.

The impedance meter measures the impedance "viewed" by the JFET, the tracks at the diode place are short-circuited. This schematic measurement is presented in Fig. 7. Subsequently the impedance meter is placed at the diode place, the tracks at the JFET level are short-circuited.

Finally, the equivalent impedance at the level of the 50Ω resistor inside the LISN is measured, the active components replaced by an open-circuit and by an short-circuit.

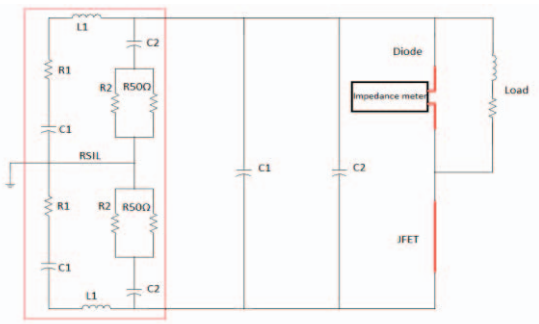

Fig. 7 Measuring schema to validate the model of passive elements

The comparison of the results for the configuration of the fig.7 is presented in (Fig. 8). All measurements show good agreement between the models and the measurements. It can be considered that the model of passive elements is valid for a wide frequency-range (40Hz to 30MHz). The approach of passive and parasitic components is then valid for predicting conducted disturbances.

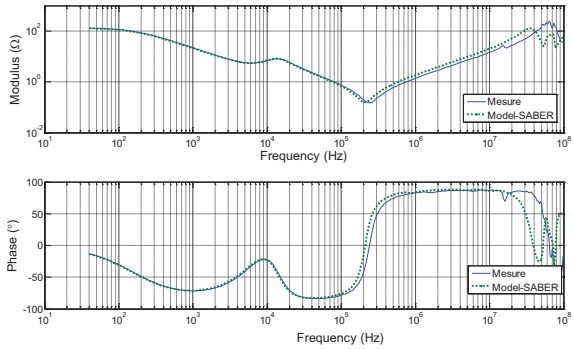

Fig. 8 Equivalent impedance measured and modeled

After a validation of impedance model, the complete model of the converter is simulated in the Saber® environment (Fig 9) in the time domain to take into account the non linear behavior of the SiC JFET and Si diode.

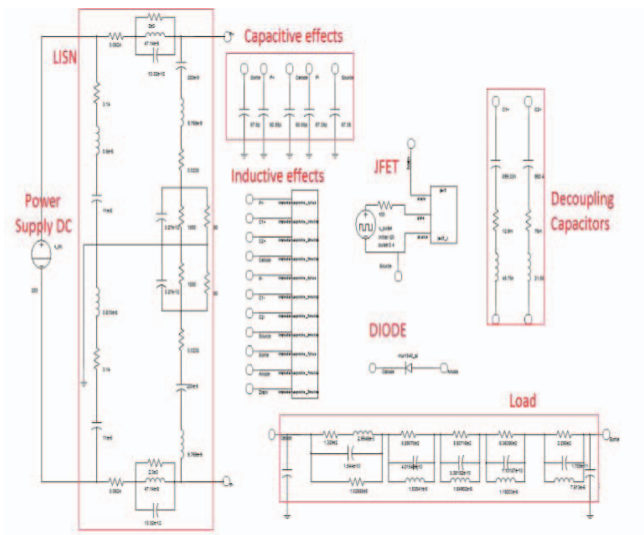

Fig. 9 Converter Saber® circuit and LISN

B. Simulated spectrum of electromagnetic interferences compared with measurements.

The spectrum presented in Fig. 10 comes from FFT results given by the experimental data measured in time domain with an oscilloscope (LeCroy HRO 66Zi) and compared to Saber model results (FFT with Matlab of time domain numerical results).

These measurements are made at the 50 ohms resistor of the LISN. It can be considered that the model is valid up to 20 MHz (Fig. 10).

A new characterization of semiconductor components must be performed to increase the frequency validity range of the whole model. Indeed, because of the impedance model frequency validity, it is clear that the differences observed on the results come from the semiconductor components models (JFET and Diode).

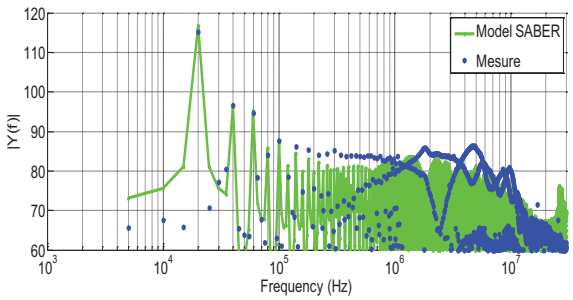

Fig. 10 Measured and modeled EMI spectrum

IV. Conclusion

A method to take into account stray elements in a power converter has been presented. The impedance model is valid up to a frequency of 30 MHz.

The complete model of the converter (passive components, stray elements, SiC and Si components) was simulated in the Saber® environment in time domain and confronted with measurements. This model allows forecasting the conducted EMI spectrum up to 20 MHz.

Future work will be dedicated to the semi-conductor components model characterization to increase the validity range. A sensibility study will be proposed in the different ranges of frequency to quantify the importance of each component (passive elements, parasitic elements, SiC and Si model devices) involved in the converter in the conducted perturbations. Comparisons of the interferences between SiC and Si components were carried out; results are presented in [9].

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V. References

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